REMARKS

Claims 1-4, 6-10, 12-27, and 29-39 are pending. Claims 1, 12, 27, and 29 have been amended, claims 5, 11, and 28 have been canceled, and new claims 31-39 have been added to recite additional features of Applicant's invention. Claims 14, 17, 21, 25, and 26 have been indicated to be allowable.

Reconsideration of the application is respectfully requested for the following reasons.

In the Office Action, the Examiner rejected claims 1-6, 8, 9, 12, 13, 15, 16, 18-20, 22-24, 27, and 28 under 35 USC § 102(e) for being anticipated by the Forbes patent publication. This rejection is traversed for the following reasons.

Claim 1 has been amended to recite that the floating body is "reset when the second control signal assumes a first value, the first value being lower than a second value which the second control signal assumes when the data is written into the floating body." In addition to these features, claim 1 recites that the "first channel interface is a drain and the second channel interface is a source of the transistor." The Forbes publication does not disclose these features.

The Forbes publication discloses a memory cell having a transistor with a floating body. During a write operation, the floating body stores a logical value corresponding to the voltage on the bit line. This operation is preceded by a reset operation, which involves forward-biasing a drain-body junction to remove any residual body charge. See Paragraph [0014].

The Forbes publication, however, does not disclose the invention defined in claim 1. Claim 1, for example, recites that the drain of the transistor receives the data signal and that the source of the transistor receives the second control signal. The reset (or purge) operation is then performed when the second control signal (which is input into the source) assumes a first value.

Moreover, claim 1 recites that the first value is lower than a second value which the second control signal assumes when the data is written into the floating body. These additional features are not disclosed in Forbes. Neither are they inherent to the memory cell disclosed Forbes under the standard set forth in MPEP § 2112 et seq. Under § 2112, claim features are inherent only when they are *necessarily present* in a reference. In the present case, "the first value is lower than a second value which the second control signal assumes when the data is written into the floating body" are not necessarily present in Forbes for purposes of performing its reset operation.

Because the Forbes publication does not disclose all the features recited in claim 1, Forbes cannot anticipate this claim. It is therefore submitted that claim 1 and its dependent claims are allowable.

Claim 27 recites that "the first set of control signals and the second set of control signals being received at a gate of the transistor and a source of the transistor, and the data signal is received at a drain of the transistor." This claim further recites: "the first set of control signals including a purge signal coupled to the source of the transistor, the purge signal having a first value lower than a second value which is coupled to the source when the data is selectively written to the floating body of the transistor." (Emphasis added). The Forbes patent does not explicitly or inherently disclose these features. Accordingly, it is submitted that claim 27 is allowable.

Claim 29 recites features similar to those which patentably distinguish claim 1 from the Forbes publication. It is therefore respectfully submitted that claim 29 and its dependent claims are allowable.

The Examiner rejected claim 10 under 35 USC § 103(a) for being obvious in view of a Forbes-Ohsawa combination. This rejection is traversed for the following reasons.

The Ohsawa publication references a document (4) which the Examiner has relied on to reject claim 10. Document (4) corresponds to an article entitled "A Capacitorless DRAM Cell on SOI Substrate." (A copy of this article is cited in an IDS submitted contemporaneously with this paper). The article discloses a memory cell having a purge line coupled to a transistor terminal. Unlike the claimed invention, however, the purge line is coupled to the gate of the transistor, not the source as recited in claim 1. (See page 26.4.4 of the article, which provides in relevant part: "The PURGE operation is to expel the electrons out of the floating body. It can be done by raising the floating body potential (by applying a negative voltage to WL) . . ."

Modifying Forbes with the Ohsawa publication would therefore produce a memory cell having a purge line coupled to a gate of a floating-body transistor, not to the source as recited in the claims. It is therefore submitted that a Forbes-Ohsawa combination would fail to form the invention defined in claim 1, and that claim 10 is allowable at least by virtue of its dependency from claim 1.

The Examiner rejected claim 7 under 35 USC § 103(a) for being obvious over Forbes taken alone and claims 29 and 30 for being obvious in view of a Forbes Gomes combination. The Gomes publication was cited for its disclosure of off-chip cache memories. Gomes does not teach or suggest the features of claim 1 missing from the Forbes publication, and therefore it is submitted that claims 7, 29, and 30 are allowable at least by virtue of the features recited in their base claims.

New claims 31-39 have been added to the application.

Claim 31 recites that the first and second voltage levels recited in claim 17 are a same voltage level. These features are not taught or suggested in the cited references, whether taken alone or in combination.

Claim 32 recites a memory cell, comprising a transistor which includes a gate coupled to a word line, a drain coupled to a bit line, a source coupled to a purge line, and a floating body between the source and drain. This claim further recites that the purge line assumes a first value during a reset operation and a second value when data is stored in the floating body during a write operation, the first value being lower than the second value. These features are not taught or suggested in the cited references, whether taken alone or in combination.

Claim 33 recites that "the word line assumes the first value and the bit line assumes the second value during the reset operation." These features are not taught or suggested in the cited references, whether taken alone or in combination.

Claim 34 recites that "the first value lies in a negative voltage range." These features are not taught or suggested in the cited references, whether taken alone or in combination.

Claim 35 recites that "the negative voltage range includes -0.5 V. to -2.5V." These features are not taught or suggested in the cited references, whether taken alone or in combination.

Claim 36 recites that "the word line and purge line assume the second value and the bit line assumes the second value or a greater value during a hold operation." These features are not taught or suggested in the cited references, whether taken alone or in combination.

Claim 37 recites that "the bit line assumes the second value and the word line assumes a third value during the reset operation, the first value and the third value both included in a

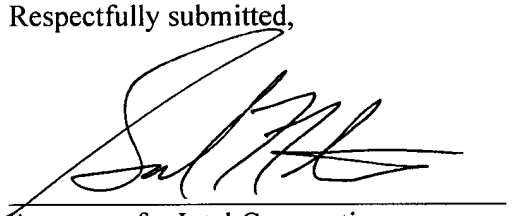
negative voltage range." These features are not taught or suggested in the cited references, whether taken alone or in combination.

Claim 38 recites that "the negative voltage range includes -0.5 V to – 2.5V." These features are not taught or suggested in the cited references, whether taken alone or in combination.

Claim 39 recites that "the first and third values are a same value." These features are not taught or suggested in the cited references, whether taken alone or in combination.

In view of the foregoing amendments and remarks, it is respectfully submitted that the application is in condition for allowance. To the extent necessary, Applicants petition for an extension of time under 37 CFR § 1.136. Please charge any shortage in fees due in connection with this application to Deposit Account No. 16-0607 and credit any excess fees to the same Deposit Account.

Respectfully submitted,



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